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Design of a High frequency Hysteresis-Controlled CMOS Buck Converter for low power Applications

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ABSTRACT: This paper presents the design of a 20 MHzhysteresis-controlled CMOS buck converter using pseudo ramp techniques for ultra-low power applications. The proposed buck converter can improve the transient response using hysteresis-controlled and fixed-voltage band techniques. Using pseudo ramp technique, pseudo inductor current signal can be produced to reduce the output voltage ripple. At the same time, the sub-1-V structure leads to low power dissipation. Moreover, by adopting the inverter-based low-voltage error amplifier topology, the proposed buck converter becomes most suitable for the low-power applications.The prototype of buck converter has been designed with 180nm 2P3M CMOS technology. The operating frequency of proposed converter is 20 MHz, with an inductor of 8.5 μH and a capacitor of 330 nF. Experimental results show that the output voltage is 0.5 V, the load current is 27 mA.

Keywords: Buck converter, hysteresis-controlled techniques, CMOS, pseudo ramp signal generation.

I. INTRODUCTION

Today's electronic systems are designed with advanced manufacturing processes as there is a rapid growth in CMOS technology, in which low supply voltage is very essential.The development of CMOS technology is continued due to the need for portable applications involving low-voltage single-cell battery operations, including ADC, SRAM and filter modules are to be operated at a low supply voltage of less than 1 V. To adopt such a low-voltage environment, many literatures have been proposed [1]-[6]. These advanced VLSI systems imposes new challenges on power supply design like improving stability and reliability, because the circuits are more sensitive to noise, such as overshoot and undershoot present in the supply. However, the conventional DC-DC converters with the transient response of below 100 μs are available for 3.3/5 V applications. But, for sub-1-V applications, the quality of response should be enhanced to achieve transient response of below 10 μs.

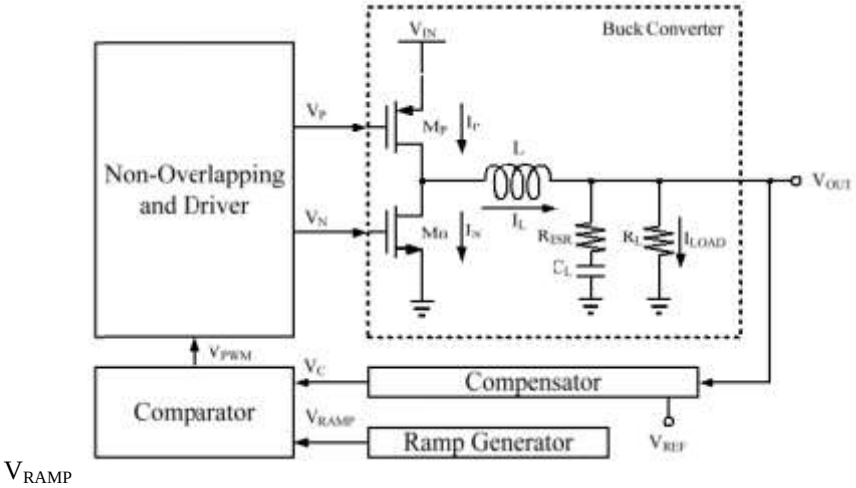
There are various control schemes are available and hybrid control schemes are also present to design a buck converter. However, the popular fast-response of the controlled scheme involves hysteresis control. Types of hysteresis control are voltage-mode hysteresis control [7]-[9], current-mode hysteresis control [10]-[12] and digitalized hysteresis control [13]-[15].A hysteresis current-controlled buck converter achieves high speed transient response because of the current signal transfer and also enhanced stability due to phase locked loop circuit, used to adjust the switching frequency, but the current transfer path reduces the power efficiency[12]. The digital controlling technique has a major drawback due to computational time delay coming from analog to digital conversion, algorithm computation and pulse width modulation generation in the control loop. The digital controller of [14] reduced this time delay by eliminating one switching cycle time delay.

In this paper, a voltage-mode hysteresis control scheme is proposed for fast-transient response. In the voltage-mode hysteresis controlled design, a large equivalent series resistance (ESR) of the output capacitor is used to obtain the inductor current message signal and modulate the system. The large ESR causes two effects in general, first is, it improves the accuracy by minimizing the phase delay and the second is undesired effect, leads to non smoothness of circuit. A large output voltage ripple would affect the accuracy, even in steady state. So, a large ESR is not suitable, especially for low-voltage applications. If a small ESR is designed to reduce the output ripple, it can improve the transient period and steady state, but it may not work properly in the conventional hysteresis control. Other current sensing schemes are developed to obtain fast-transient response without requiring large ESR, but they are involved with complicated circuit. Under large ESR conditions, a more precise value of current signal can be sensed, but it would sacrifice the stability.

It is the typical concern for the proposed circuit to deal the trade-offs between ESR value and the inductor current message signal. Also, the circuit id designing for ultra low power applications,this corresponding consideration should be taken. Based on these considerations, a new hysteresis controlled buck converter is designed to tackle the issues using a pseudo ramp generator.

II. VOLTAGE-MODE PWM CONTROL

The block diagram of voltage-mode PWM control is shown in Fig.1. The non-overlapping and driver circuit prevents the PMOS and NMOS transistors from shorting and drive them efficiently. The PMOS and NMOS transistors acts like switches. The inductor and capacitor are used to construct a filter. Whenever the PMOS transistor conducts, the current $I_P$of PMOS equals to the inductor current and this current increases in a certain positive slope according to the inductor value and output voltage signal. The output voltage is fed into compensator to generate the compensated signal V_C.When the ramp signal



V_{RAMP}

Fig. 1. Simplified structure of voltage-mode PWM control.

becomes higher than compensated voltage V_C, the comparator generates V_{PWM} as high. Similarly, V_{PWM} can produce both V_P and V_N signals.They can be high to tur off the high-side PMOS transistor and turning on the low-side NMOS transistor until the next clock pulse through the non-overlapping and driver.

III. HYSTERESIS CONTROL-PSEUDO RAMP TECHNIQUE

The proposed buck converter with hysteresis control scheme using pseudo ramp techniue is shown in Fig. 2. The proposed buck converter has two feedback loops. The inner loop consists of pseudo ramp generaror to generate the voltage signal V_S, which resembles the inductor current signal. The outer loop paasses through the compensator, fixed

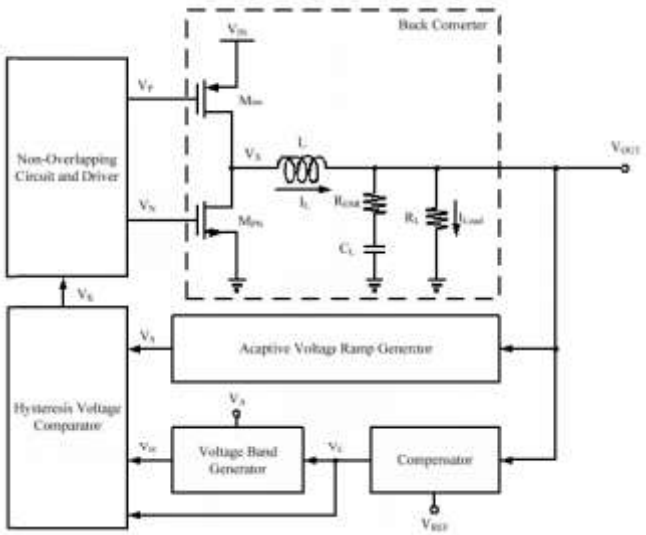


Fig. 2. Block diagram of proposed hysteresis-controlled buck converter using pseudo ramp technique.

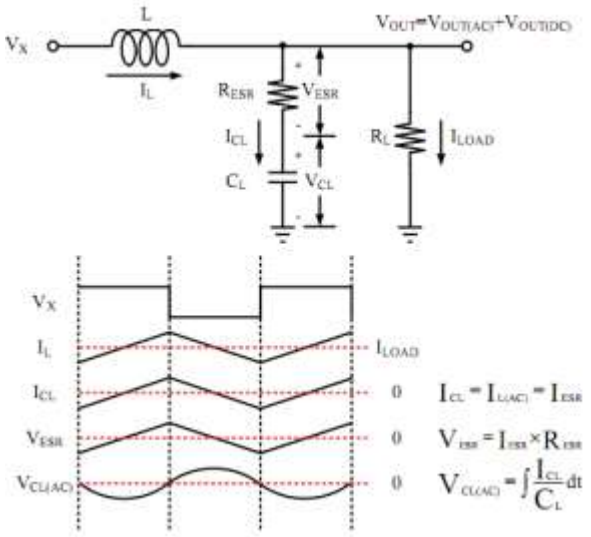


Fig. 3. Output filter of buck converter.

voltage band generator and hystresis comparator. The output voltage is fed into the compensator with reference voltage V_{REF} to generate compensated signal V_C. The fixed band generator adds an analog voltage V_A to obtain the signal V_H. The signals V_H and V_C forms the hysteresis level and the pseudo ramp signal V_S is applied to the hysteresis comparator. Finally, the digital signal V_K is generated by the hysteresis comparator and it caan be used to generate the V_P and V_N signals. The non-overlapping and driver circuit avoids the transistors from shorting and drives them efficiently.

By direct analysis, we can obtain the voltage riple as

(1)

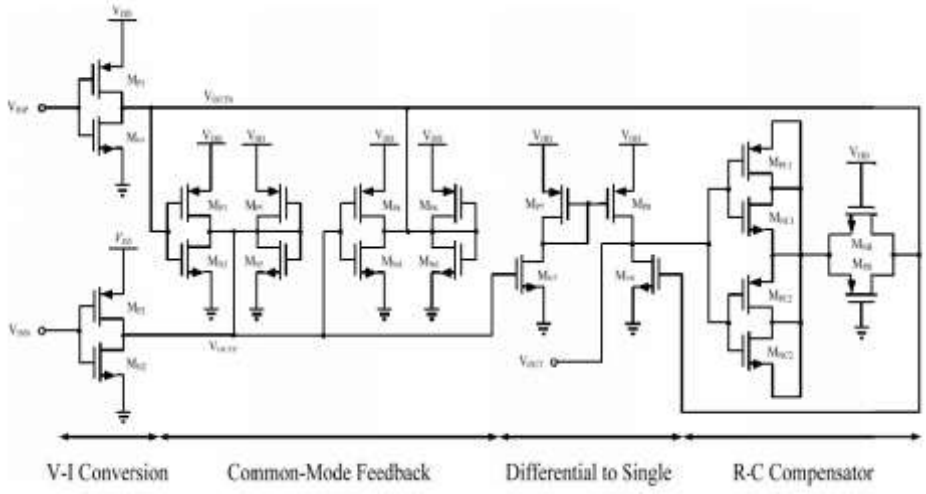


Fig. 4. Low-voltage operational error amplifier.

Based on this equation, the output ripple can be minimized by increasing the switching frequency or using a small capacitor. The ouput filter of the buck converter is shown in Fig. 3. $V_{CL(AC)}$ is a part of the AC signal of the inductor current on the output capacitor. When V_X is high, the inductor current increases and $V_{CL(AC)}$ will ramp up. When V_X is connecting to the ground, inductor current and $V_{CL(AC)}$ will ramp down. The ESR is necessary to obtain proper inductor current sensing, but it will cause large output ripple, which affects accuracy. To overcome this problem, in this proposed converter, a pseudo ramp generator is used to produce a ramp which is similar to inductor current signal without using a large ESR of output capacitor.

A. Pseudo Ramp Generator

As shown in Fig. 4, the inverter-based low-voltage error amplifier consists of CMOS inverters in its V-I conversion stage[24]. The class AB operation of CMOS inverters results in low power consumption. Hence, this inverter-based low-voltage operational amplifier is most suitable to operate under 1 V with low power and high gain. The CMOS inverter has a favourable linearity when the PMOS and NMOS transistors are matched

with each other. The signal amplification is carried out by two matched inverters M_{P1} - $M_{N1}$and M_{P2}- $M_{N2.}$ Additionally, the common-mode feedback (CMFB) part is composed of inverter-based latch. The group inverters M_{P5}-M_{N5} and M_{P6}-M_{N6} are diode-connected resistances between the output nodes (V_{OUTP}/V_{OUTN}) and the common-mode voltage level. The other group inverters M_{P3}-M_{N3} and M_{P4}-M_{N4} inject the output

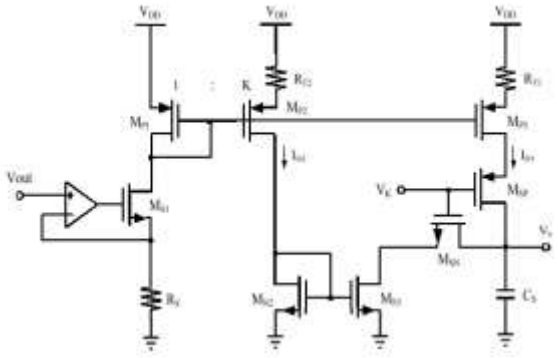
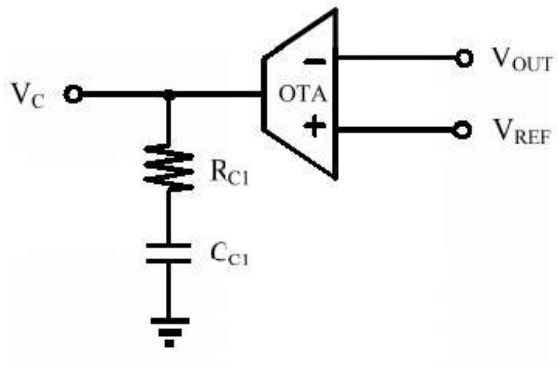
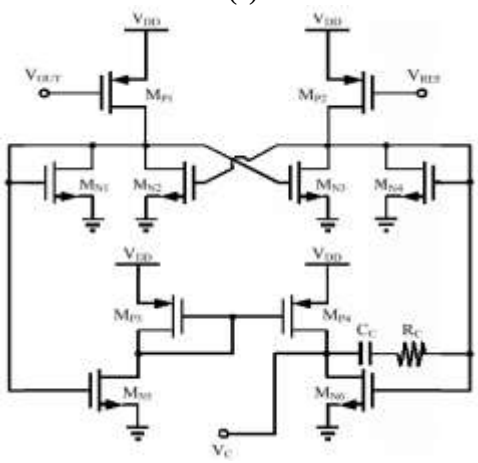


Fig. 5. Pseudo ramp generator.

currents into the diode-connected resistances. Thus, they become virtual loads at the output nodes. As the two group inverters having the same supply, the transconductance, $g_m$is equalin every group inverter. Hence, the CMFB part is operated at low-ohm load situation.The common-mode voltage level is decided by four matched inverters from M_{P3}-M_{N3} to M_{P6}-M_{N6}. In DC part, the $M_{N,P5}$ and $M_{N,P6}$ operates in saturation region and maintains the DC voltage at the half supply voltage to achieve the highest output swing in output differential signals. In AC part, the part of the CMFB $M_{N,P3}$and $M_{N,P4}$ have gain for the amplifier. We choose $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$, and $g_{m3} > g_{m5}$; the width of the transistors of M_{P5}-M_{N5} and M_{P6}-M_{N6} are designed to be slightly smaller than those ofM_{P3}-M_{N3} and M_{P4}-M_{N4}. Finally, the inverter-based low-voltage error amplifier that consists of six CMOS inverters has a large bandwidth because of the simple structure. The R-C compensation can provide the stability of amplifier with zeros and poles andthe



(a)



(b)

Fig. 6. (a) Schematics of OTA. (b) Detail circuit.

differential-to-single circuit uses a single-stage differential amplifier with an active current mirror load. It causes the dual outputs to transfer into a single-ended output.

The pseudo ramp generator is as shown in Fig. 5. [27]. The feedback network decides the reference current I_S via V_{out} and R_S to charge or discharge the capacitor C_S. The currents of the $I_{D1,\ 2}$ of the pseudo ramp generator can be described as,

where I_S equals to V_{out} divided by R_S, and $I_{D1}$and I_{D2}equal to K times $I_S$when the trimming resistance equal to zero. The signal $V_K$is produced by comparing the signal of the pseudo ramp generator $V_S$with the voltage band formed byV_H and V_C. The signal $V_K$from the hysteresis comparator controls the operation of charging and discharging. The slope of the pseudo-inductor current signal, which is in phase with the inductor current. The equation of the pseudo-inductor current is as follows:

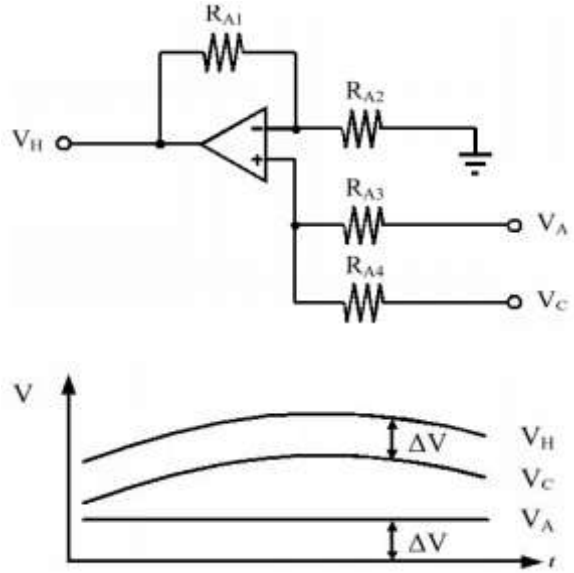


Fig. 7. Fixed band generator.

B. Compensator

Fig. 6. Shows the schematics of the operational transconductance amplifier (OTA) circuit. This circuit can generate poles and zeros to cancel the inherent poles and zeros in the buck converter.Adopting a PI compensator can generate a dominant pole and high gain at the low frequency, since the large capacitor C_{C1} at the OTA output is used to achieve the dominant pole compensation. Therefore, the large signal is very poor. After increasing R_{C1}, the zero of the compensation resistance increases the phase margin at the middle-frequency, and the large signal response of V_C becomes more elastic.

C. Fixed Band Generator

The fixed band generator is shown in Fig. 7. The voltage V_A, the analog voltage, which is generated by the voltage divider of V_{in}. The signal V_C adds V_A to get a precise voltage value VH when resistors RA1, RA2, RA3, and RA4 are identical. VH varies with the VC when VC changes with the output.

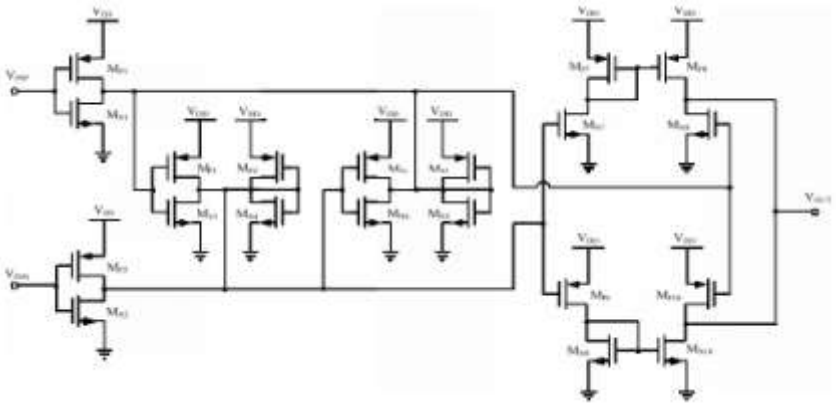


Fig. 8. Comparator

D. Hysteresis Comparator

As shown in Fig. 8, the comparator circuit is composed of digital components. The low-voltage comparator circuit has three subparts. The first part is gain amplifier circuit, which consists of two matched CMOS inverters. CMFB circuit is the second stage.

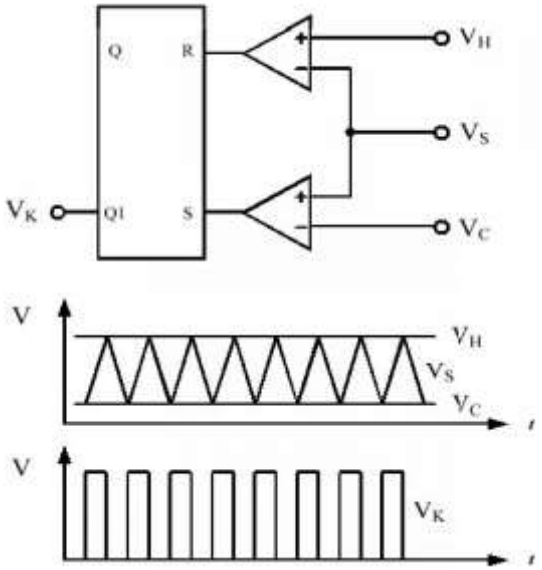


Fig. 9. Hysteresis comparator.

The third stage consists of two voltage-to-current converters, which are n-type and p-type. Two types of current converters decrease the input-referred offset by using a complementary structure. Finally, the digital comparator has the advantages of single-ended output and full rail-to-rail swing, wider than the conventional structures in low-voltage applications.

Fig. 9. presents the hysteresis comparator circuit with two low-voltage comparators and J-K flipflop to produce the hysteresis range with the upper limit as V_H and the lower limit as V_C. It limits the signal VS to produce two signals into the J-K flipflop, to generate the square wave signal V_K. The hysteresis-voltage-controlled method provides the architecture to achieve fast transient responses. The switching frequency is determined by the signals V_H and V_C. When V_S is higher than V_H, V_{DUTY} is high, and vice versa.

Fig. 10. Waveforms of V_{out} and $I_{L.}$

IV. EXPERIMENTAL RESULTS

The proposed hysteresis-controlled CMOS buck converter using pseudo ramp technique was designed with 0.18 µm CMOS technology. The measured waveform of the output voltage, which includes $V_{out}$and inductor current IL, is shown in Fig. 10, and the switching freuency is 20 MHz. Fig. 11. shows the pseudo ramp generator output VS and inductor current IL. As shown in Fig. 11. The signal VS is in phase with inductor current IL.

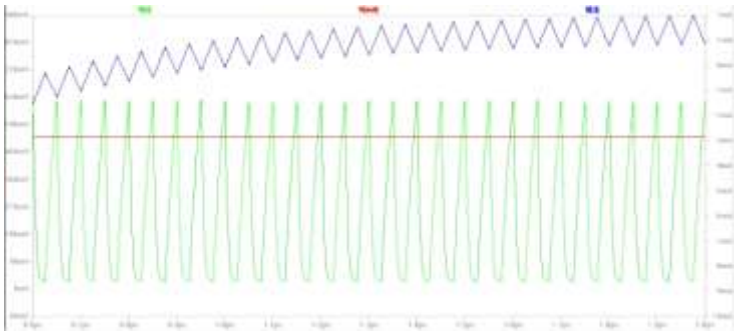


Fig. 12. Transient response when the load current chenges with supply voltage and output voltage.

Fig. 12. Transient response.

TABLE I: SUMMARY OF PERFORMANCE

Technology	0.18 μm 2P3M
Input voltage	1 V
Output voltage	0.5 V
Inductor	8.5 μH
Capacitor	330 nF
Operating frequency	20 MHz
Maximum Load current	2 mA
Output voltage ripple	0.00008
Transient response	
Maximum efficiency	63.5 @ 25 mA

Parameter	[8]	[28]	[29]	This paper
Technology [μm]	0.35	0.13	0.5	0.18
Inductor [μH]	4.7	0.00082	0.27	8.5
Capacitor [μF]	10	0.02	1.6	0.33
Input [V]	3	1.2	2.7-5.5	1
Output [V]	0.5-2.5	0.4-0.96	1.2	0.5
Frequency [MHz]	0.85	90-240	20	20
Output ripple [mV]	N.A.	25	4	
Maximal load current [mA]	500	240	600	320
Maximal efficiency [%]	94.5 @ N.A.	80 @ 200 mA	84.5 @ 250 mA	

The measured performance summary of the proposed buck converter is given in Table I. in this design, the supply voltage is 1 V. In Table II, the proposed converter is compared with the state-of-the-art circuits [8], [28], [29]. In [8], the switching frequency is approximately 850 kHz, and off-chip inductor and output capacitor are 10 μH and 4.7 μF, respectively.

V. CONCLUSION

The proposed 20 MHz hysteresis-controlled CMOS buck converter using pseudo ramp techniques is designed with 0.18-μm 2P3M CMOS processes. The pseudo ramp generator effectively solves the large output ripple problem with large ESR capacitor. The proposed buck converter demonstrates an extremely fast transient response and high efficiency at 1-V supply voltage. Compared with conventional buck converters, this design has the major advantages, including fast response, low number of components, low power supplies, and simple circuit structure for design and implementation.

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